REMARKS

As a preliminary matter, the Examiner has objected to claims 1, 12, 13, 16, 19, 22, 25, 26, and 28 because of various informalities. Accordingly, Applicants have amended claims 1, 12, 13, 16, 19, 22, 25, 26, and 28 to correct these informalities. Therefore, Applicants respectfully assert that claim 1, 12, 13, 16, 19, 22, 25, 26, and 28 are now in acceptable form.

In addition, the Examiner has rejected claims 3, 4, 12-20, 22, and 25-28 under 35 U.S.C. § 112, second paragraph, as lacking antecedent basis for various terms. The Examiner has also rejected claims 19-31 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. The Examiner has rejected claims 1-6, 9-15, 18-19, and 23-26 under 35 U.S.C. § 102(b) as being anticipated by SU 1619279 to Ulybin ("Ulybin"). The Examiner has also rejected claims 7 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Ulybin in view of U.S. Patent No. 5,079,496 to Pierret et al. ("Pierret"). In addition, the Examiner has objected to claims 8, 17, 20-22, and 27-31 under 35 U.S.C. § 103(a) as being unpatentable over Ulybin in view of U.S. Patent No. 5,079,496 to Aslin et al. ("Aslin"). Claims 1, 3, 4, 12-14, 16, 18-20, 22, and 25-28 have been currently amended. Claims 1-31 are currently pending. The following remarks are considered by applicant to overcome each of the Examiner's outstanding rejections to current claims 1-31. An early Notice of Allowance is therefore requested.

I. SUMMARY OF RELEVANT LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The determination of obviousness rests on whether the claimed invention as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. In determining obviousness, four factors should be weighed: (1) the scope and content of the prior art, (2) the differences between the art and the claims at issue, (3) the level of ordinary skill in the art, and (4) whatever objective evidence may be present. Obviousness may not be

established using hindsight or in view of the teachings or suggestions of the inventor. The Examiner carries the burden under 35 U.S.C. § 103 to establish a prima facie case of obviousness and must show that the references relied on teach or suggest all of the limitations of the claims.

II. REJECTION OF CLAIMS 3, 4, 12-20, 22, AND 25-28 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

On page 3 of the current Office Action, the Examiner has rejected claims 3, 4, 12-20, 22, and 25-28 under 35 U.S.C. § 112, second paragraph, as lacking antecedent basis for various terms. This rejection is respectfully traversed and believed overcome in view of the following discussion.

Applicants have amended claims 3, 4, 12-20, 22, and 25-28 so as to provide the requisite antecedent basis for the various terms. More specifically, Applicants have (1) amended references to "the system" in claims 3-4, 12-13, 19-20 and 26-28 so that they now refer to "the electronic system"; (2) amended claims 3, 12, 19 and 26 so that they now firstly recite "a generation", instead of "the generation", and secondly recite "the generation" instead of "generation"; (3) amended claims 14 and 18 so that they now depend from claim 10 instead of claim 1; (4) amended claims 20 and 22 so that they refer to "a processor" instead of "the processor"; and (5) amended claim 25 so that is refers to "electronic system" instead of "electronic signal".

Therefore, Applicants respectfully assert that claims 3, 4, 12-20, 22, and 25-28 are now in acceptable form, and respectfully request the Examiner remove the rejection of claims 3, 4, 12-20, 22, and 25-28 under 35 U.S.C. § 112, second paragraph.

III. REJECTION OF CLAIMS 19-31 UNDER 35 U.S.C. § 101

On page 4 of the current Office Action, the Examiner rejects claims 19-31 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject

matter. This rejection is respectfully traversed and believed overcome in view of the following discussion.

The Examiner asserts that:

> Claims 19-31 appear to be directed to an abstract idea rather than a practical application of an abstract idea which would produce a "useful, concrete, and tangible result." For example, claims 19 and 26 are merely directed towards storing a record and generating a signal, which may not be held to be a tangible result, and therefore non-statutory subject matter. This claimed subject matter lacks a practical application of a judicial exception since it fails to produce a useful, concrete and tangible result. Office Action (3/28/07), P. 4.

This, however, misinterprets independent claims 19 and 26.

Claims 19-25

Claims 19 states, in part, that the claimed invention is "arranged to ... generate an alarm signal." Applicants respectfully assert that the generation of an alarm signal is a useful, concrete, and tangible result. In particular, the alarm signal is a concrete and useful way to test fault monitoring systems in vehicles to ensure the fault monitoring systems are operating correctly. Application (as filed), P. 1, Lns. 3-17.

Accordingly, Applicants respectfully assert that Examiner has failed to establish a prima facie case that independent Claim 19, and corresponding claims 20-25 because they are all dependant from independent Claim 19, are directed to non-statutory subject matter. Therefore, Applicants respectfully request that Examiner remove the rejection of claims 19-25 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Claims 26-31

Claims 26 states, in part, that the claimed invention is a "method comprising ... generating an alarm signal." Applicants respectfully assert that the generation of an alarm signal is a useful, concrete, and tangible result. In particular, the alarm signal is a concrete and useful way to test fault monitoring systems in vehicles to ensure the fault monitoring systems are operating correctly. Application (as filed), P. 1, Lns. 3-17.

Accordingly, Applicants respectfully assert that Examiner has failed to establish a prima facie case that independent Claim 26, and corresponding claims 27-31

because they are all dependant from independent Claim 26, are directed to non-statutory subject matter. Therefore, Applicants respectfully request that Examiner remove the rejection of claims 19-25 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

IV. REJECTION OF CLAIMS 1-6, 9-15, 18-19, AND 23-26 UNDER 35 U.S.C. § 102(B) BASED ON ULYBIN

On page 4 of the current Office Action, the Examiner rejects claims 1-6, 9-15, 18-19, and 23-26 under 35 U.S.C. § 102(b) as being anticipated by Ulybin. This rejection is respectfully traversed and believed overcome in view of the following discussion.

Ulybin does not disclose all of the elements of independent claims 1 and 10. Specifically, Ulybin discloses fault simulation systems, not fault monitoring systems. Further, Ulybin does not disclose "a plurality of fault monitoring systems each of which is adapted to output a fault signal when an input indicates that the electronic system is in a fault condition associated with the fault-monitoring system", or that "a fault signal output from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault-monitoring systems to simulate a fault condition associated with the subsequent fault-monitoring system".

Firstly, referring to Figures 1 and 2 of the Ulybin document, the fault simulating systems (20) in Ulybin do not output a fault signal "when an input indicates that the electronic system is in a fault condition". Instead, the fault simulating systems (20) generate fault signals on their output (13) so as to attempt to cause a fault condition in a computer system under test. In addition, in Ulybin, the fault condition is not associated with the fault simulating system, instead it is associated with the computer system under test.

Secondly, in Ulybin, the fault signal output (13) is not provided as an input to a subsequent fault simulating system. Instead, in Ulybin, the fault signal output (13) from the last module is fed into an input (14) of the first module, not into a subsequent fault simulating system, as can be seen in Figure 2. Furthermore, in Ulybin, this is not done to simulate a fault condition associated with the subsequent fault simulating system. Ulybin is instead concerned

with injecting fault simulation pulses into a computer system under test in order to simulate fault conditions in the computer system under test. Independent claims 1 and 10 of the present invention are therefore novel over the disclosure of the Ulybin document.

Ulybin does not disclose all of the elements of claims 19 and 26. Specifically, Ulybin does not disclose "store[ing] a record ..... in non-volatile memory", or "on subsequent reversion of the system to a non-fault condition, check[ing] whether the non-volatile memory includes a record of a first fault signal and when the non-volatile memory does not include a record of such a first fault signal on subsequent reversion, generat[ing] an alarm signal"

Firstly, non-volatile memory is commonly understood to be memory which retains its contents after removal of the power supply to that memory element. It is important to recognize that Ulybin has been translated by machine into English which has resulted in a rather literal translation of certain words. By reading the disclosure in context however it is clear that the "trigger" (4) in Ulybin is a memory element having a "record" (clock) input, a reset input, an input 12 by which information may be "recorded to" the "trigger" (a data input), an output showing the stored, or recorded, information and an "inverse output" (showing the inverse of the stored, or recorded, data). A person skilled in the art would immediately recognize the trigger element 4, by its characteristic controls, as being a D-type flip flop which is very commonly used in digital logic circuits of the type described in the Ulybin document. A person skilled in the art would know that D-type flip flops implemented in common semiconductor processes require a power supply, do not retain their contents when the power is removed and are therefore classed as volatile memory. In any case, Ulybin does not mention or hint at non-volatile memory, either by name or by reference to its properties.

Secondly, Ulybin does not identify an alarm condition. Ulybin does not identify either the occurrence of a Comparator match or the extended non-occurrence of a comparator match to be an alarm condition, nor is there any mention that an alarm is signaled. Independent claims 19 and 26 are therefore novel over the Ulybin disclosure.

A more detailed description of the way that Ulybin operates follows in order to illustrate the points made above. Considering the purpose of the daisy-chained signals

disclosed in Ulybin which are carried between outputs 17 and inputs 15 of modules 20, each of the fault simulating system modules 20 compares the state of the fault tolerant computer system under test ("the address, page register, command counter" - page 6, line 12) with the contents of counter 1. If comparator 3 detects a match, then a fault simulation pulse is produced on output 13 (page 3, lines 11-13). If a match doesn't occur for a period of time (the "extended non-occurrence of the tracked condition", page 10, lines 18-19) then counter 2 will overflow, causing counter 1 to increment (page 10, second paragraph). When counter 1 overflows ("after the fault is set in all micro commands"), output 17 is asserted (page 14, line 8). This is connected to input 15 of the subsequent daisy-chained fault simulating system and is passed via OR gate 6 to counter 1, having the effect of incrementing counter 1 of the subsequent module in the daisy-chain (page 14, lines 13-15). Since comparator 3 compares counter 1 output with state information from the computer system under test, this has the effect of changing the point at which errors are injected so as to simulate faults in the computer system under test. The signals daisy-chained from outputs 17 to inputs 15 are therefore associated with simulation of faults in the computer system under test, not with simulation of a fault condition associated with the subsequent fault simulation system.

Referring to the other daisy-chained signals disclosed in Ulybin, carried between outputs 16 and inputs 14 of the modules 20, input 14 is the reset input of a D-type Flip-Flop 4 (page 9, lines 9 - 11). The inverting output 16 of the Flip-Flop 4 goes high when the flip-flop is reset and retains this state until a match is detected by the comparator 3. This output 16 is then daisy-chained into the subsequent module's input 14 (which is the reset input of the flip-flop 4 in the subsequent module). Thus, the flip flops in the subsequent modules are held in reset so that they do not produce fault simulation pulses on output 13 ("the low potential is transmitted from output 13" - page 9, lines 11-12). At the same time, AND gate 8 in the subsequent module is "blocked" (page 9, lines 21-22) with the effect that the clock to counter 2 in the subsequent modules is inhibited (page 10, lines 3-9). Thus, initially, only the first module in the chain is initially permitted to operate and produce fault simulation pulses. Later, when comparator 3 detects a match, the flip flop 4 stores a binary '1' digit which has the effect that output 16 goes low and subsequent modules in the chain are

then permitted to begin operating (page 10, lines 22-24 & page 11, lines 7-13). The signals daisy-chained from outputs 16 to inputs 14 therefore control the simulation of fault conditions in the computer system under test and have nothing to do with simulation of a fault condition associated with the subsequent fault simulation system.

Neither the Pierret Patent (US5079496) nor the Aslin Patent (US4943919) discloses all of the elements of the independent claims of the present application.

Pierret does not disclose that "fault-monitoring systems are arranged in a cascade fashion such that a fault signal output from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault-monitoring systems to simulate a fault condition associated with the subsequent fault-monitoring system". Pierret describes voltage monitoring and regulation apparatus. The voltage monitoring apparatus is not arranged in cascade and the output of the voltage monitoring apparatus is not used as an input to further voltage monitoring apparatus in order to simulate a fault with the voltage monitoring apparatus. Present invention claims 1 and 10 are therefore novel over the Pierret disclosure. Pierret does not disclose storing a record of a fault in non-volatile memory. Claims 19 and 26 of the present invention are therefore novel over the Pierret disclosure.

Aslin does not disclose that "fault-monitoring systems are arranged in a cascade fashion such that a fault signal output from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault-monitoring systems to simulate a fault condition associated with the subsequent fault-monitoring system". Aslin describes an aircraft computer system used for collecting and analyzing maintenance information. In Aslin, LRU faults are collected and consolidated but are merely reported and are not input into subsequent LRUs to simulate a fault condition associated with a subsequent fault-monitoring system.

Furthermore, Aslin does not disclose "on subsequent reversion of the electronic system to a non-fault condition, check whether the non-volatile memory includes a record of a first fault signal and when the on-volatile memory does not include a record of such a first fault signal on subsequent reversion, generate an alarm signal. In Aslin, faults are

signaled when they are present in the non-volatile memory and when these faults are cleared from the non-volatile memory then no associated fault is signaled. The present invention differs in that it signals an alarm if, upon a reversion to a non-fault condition, no fault signal is recorded in the non-volatile memory. The apparatus in Aslin operates upon a different principle and therefore Aslin does not disclose the specific features of the present invention.

The independent claims of the present application are therefore novel in the light of the prior art.

As such, Applicants respectfully assert that Examiner has failed to establish a prima facie case of anticipation of independent claims 1, 10, 19, and 26, and corresponding claims 2-6, 9, 11-15, 18, and 23-25 because they are all dependant from one of independent claims 1, 10, 19, and 26. Therefore, Applicants respectfully request that Examiner remove the rejection of claims 1-6, 9-15, 18-19, and 23-26 under 35 U.S.C. § 102(b) as being anticipated by SU 1619279 to Ulybin.

V. REJECTION OF CLAIMS 7, 8, 16, 17, 20-22, AND 27-31 UNDER 35 U.S.C. § 103(A)

On page 10 of the current Office Action, the Examiner rejects claims 7 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Ulybin in view of Pierret. On page 11 of the current Office Action, the Examiner rejects claims 8, 17, 20-22, and 27-31 under 35 U.S.C. § 103(a) as being unpatentable over Ulybin in view of Aslin. These rejections are respectfully traversed and believed overcome in view of the following discussion.

The present invention solves the problem of identifying failures in fault detection circuitry before a fault which the circuitry is designed to detect goes undetected due to the fault detection circuitry being faulty itself. The present invention achieves this by cascading fault indication outputs from each successive fault-monitoring system into the next fault-monitoring system such that faults may be simulated. Advantages of this method, due to the fact that the same connections and circuitry that are used to detect real faults are used to produce simulated faults, are enhanced detection of faults in the fault monitoring circuitry (in other words a reduction in false-negatives and a reduction in undetected faults) and a

reduction in the fault-monitoring circuitry overhead. In addition, in some aspects the present invention provides for the storage of fault data in non-volatile memory and the detection of errors in the process of storing faults in that non-volatile memory, this being achieved by entering a first fault condition, monitoring for the detection of the first fault, storing the fault in non-volatile memory, then upon reversion to a non-fault condition checking for the presence of the fault record in non-volatile memory.

There is no suggestion in Ulybin that any of the circuitry in the fault-simulation devices 20 is at all unreliable or would be likely to fail. Neither is there any suggestion of undesirable consequences if any of the modules 20 were to fail such that they would no longer detect failures of the system under test. There is no consideration in Ulybin of a need to detect a fault in one of the fault simulation modules 20 so that the system might prevent a fault in the computer system under test from going undetected. There is therefore nothing in Ulybin which would lead a person skilled in the relevant art to consider the problem solved by the present invention.

Even if a skilled person had recognized the problem, Ulybin would not have appeared relevant to the above problem as Ulybin does not contemplate faults in the fault simulation circuitry itself. Even if Ulybin was studied in detail, it would not have provided any help in arriving at a solution to the above problem as it does not disclose any of the advantageous features identified in the first paragraph of this section. The present invention is therefore inventive over the Ulybin disclosure.

The Pierret Patent adds only that a fault-monitoring system may be adapted to monitor for voltage levels. This is not a limitation of the present invention and is not relevant.

The Aslin Patent does not suggest cascading fault-monitoring systems in order to simulate fault conditions associated with the subsequent fault-monitoring system in the cascade. There is no suggestion that one fault-monitoring system should feed a simulated fault signal into another in order to simulate a fault condition in the subsequent fault-monitoring system.

Neither does Aslin teach that an electronic system should be placed into a first fault condition, then a first fault signal from a first fault-monitoring device should be

monitored for, then a record to this effect should be stored in non-volatile memory and finally upon reversion to a non-fault condition a check should be made for a record of a first fault condition in the non-volatile memory and when this record does not exist then an alarm should be signaled.

The present invention is therefore inventive over the prior art documents and we respectfully request favorable re-examination.

As such, Applicants respectfully assert that Examiner has failed to establish a prima facie case of obviousness of claims 7, 8, 16, 17, 20-22, and 27-31. Therefore, Applicants respectfully request that Examiner remove the rejection of claims 7 and 16 under 35 U.S.C. § 103(a) as being unpatentable over SU 1619279 to Ulybin in view of U.S. Patent No. 5,079,496 to Pierret et al. In addition, Applicants respectfully request that Examiner remove the rejection of claims 8, 17, 20-22, and 27-31 under 35 U.S.C. § 103(a) as being unpatentable over SU 1619279 to Ulybin in view of U.S. Patent No. 5,079,496 to Aslin et al.

Based upon the above remarks, Applicant respectfully requests reconsideration of this application and its early allowance. Should the Examiner feel that a telephone conference with Applicant's attorney would expedite the prosecution of this application, the Examiner is urged to contact him at the number indicated below.

Respectfully submitted,

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